REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1-19 are pending in the application. Claims 1, 7, 8, 9 and 19 have been objected to. Claims 1-19 have been rejected. Claims 7 and 8 have been amended.

Claim Objections

In the Office Action, the Examiner objected to claims **7 and 8** because of alleged informalities. Claims **7 and 8** have been amended in order to cure these informalities.

In addition, the Examiner objected to claims 1, 9 and 19, because allegedly the terminology "non-flat" used in the claims is not supported by the specification. Applicant respectfully points the Examiner's attention to Figs. 7a through 7f and the text which describes these figures. As evident from these Figures, the erase pulses have a substantially "non-flat" voltage profile. In addition, Applicant respectfully traverses this objection, in light of the fact that the term "non-flat" is a commonly used, plain English, term which clearly applies to Figs. 7a through 7f. Applicant respectfully submits that the use of the term is entirely self defining through the common knowledge of the English language, and therefore there is no particular requirement to further define such a simple and commonly known term in the specification.

Accordingly, Applicant requests withdrawal of the objection.

CLAIM REJECTIONS

35 U.S.C. § 102 Rejections

In the Office Action, the Examiner rejected claims 1-19 under 35 U.S.C. § 102(b), as being anticipated by Chindalore et al., U.S. Patent No. 6,839,280 B1 – filed June 27, 2003. Applicant respectfully traverses the rejection of claims 1-19 due to the fact that the cited reference neither teaches nor suggests all the limitations recited in independent claims 1, 9 and 19. More specifically, all the pending independent claims include the limitation of "an **erase pulse** having a **substantially non-flat** voltage profile", where as the Examiner's reference only teaches a ***threshold voltage*** profile which is non-flat due to multiple erase cycles. As one of ordinary skill in the art should know, a threshold voltage profile is a function of program or erase pulses, it is not the pulse itself.

More specifically, independent claims 1, 9 and 19 recite:

1. "A method of erasing one or more non-volatile memory ("NVM") cells comprising: applying to the one or more NVM cells an erase pulse having a substantially non-flat voltage profile."

9. "A circuit for erasing one or more non-volatile memory ("NVM") cells comprising: an erase pulse source to produce an erase pulse having a substantially non-flat voltage profile."

19. "A system for erasing one or more non-volatile memory ("NVM") cells comprising: A NVM array, and an erase pulse source to produce an erase pulse having a substantially non-flat voltage profile."

Whereas, the Chindalore reference generally teaches:

"A non-volatile memory (30) comprises nanocrystal memory cells (50, 51, 53). The program and erase threshold voltage of the memory cell transistors (50, 51, 53) increase as a function of the number of program/erase operations. During a read operation, a reference transistor

(46) provides a reference current for comparing with a cell current. The reference transistor (46) is made from a process similar to that used to make the memory cell transistors (50, 51, 53), except that the reference transistor (46) does not include nanocrystals. By using a similar process to make both the reference transistor (46) and the memory cell transistors (50, 51, 53), a threshold voltage of the reference transistor (46) will track the threshold voltage shift of the memory cell transistor (50, 51, 53). A read control circuit (42) is provided to bias the gate of the reference transistor (46). The read control circuit (42) senses a drain current of the reference transistor (46) and adjusts the gate bias voltage to maintain the reference current at a substantially constant value relative to the cell current." (Abstract)

As is well established, in order to successfully assert a prima facie case of anticipation, the Examiner must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Applicant respectfully asserts that the Chindalore reference is not sufficient as a single prior art document for the purpose of establishing a prima facie case of anticipation. The cited reference neither teaches nor suggests every element and limitation of independent claims 1, 9 and 19. More specifically, the Applicant would like to point out to the Examiner that the cited reference teaches "*As the **program/erase threshold voltage changes with the number of program/erase cycles**, a variable read reference cell gate voltage 26 changes, thus maintaining an optimum voltage margin 28 between the **program threshold voltage** and the **erase threshold voltage***.", whereas the present Application recites in each of its independent claims "...**an erase pulse** having a substantially non-flat voltage profile.". Applicant respectfully asserts that the Examiner has misinterpreted the teachings of the cited reference, by drawing an analogy between the change in **threshold voltage** along numerous **erase cycles**, as taught in the cited reference, and the application of a non-flat **erase pulse**, recited in the present Application.

As shown so forth, the cited reference's teachings are directed to a possible result of the claimed limitations and not to the limitations themselves. Therefore, Applicant respectfully asserts that these clarifications render independent claims 1, 9 and 19 proper under 35 USC 102 and requests reconsideration and withdrawal of the rejection of claims 1, 9 and 19 and all claims dependent upon them.

Applicant notes that none of the amendments to the claims herein are in response to the above discussed prior art rejections.

In view of the foregoing amendments and remarks, all the pending claims are considered to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit account No. 50-3400.

Respectfully submitted,

Vladimir Sherman
Attorney for Applicant(s)
Registration No. 43,116

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EMPK & Shiloh, LLP
116 John St, Suite 1201
New York, NY 10038
General Phone:(212) 608-4141
Facsimile: (212) 608-4144